IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Lee et al.
Case:	19-6-4
Serial No.:	09/785,604
Filing Date:	February 16, 2001
Group:	2116
Examiner:	Thuan N. Du

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450.

Signature: Gina Maurice Date: November 8, 2005

Title: Method and Apparatus for Distributing a Self-Synchronized Clock to Nodes on a Chip

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated June 6, 2005, of claims 1-7, 9-13, and 15-17 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded on May 9, 2001 in the United States Patent and Trademark Office at Reel 011793, Frame 0652, and an assignmentt under 37 CFR 3.73(b) filed on April 14, 2003. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

A Notice of Appeal was filed on July 13, 2005 in related United States Patent Application Serial No. 09/788,582 (Attorney Docket No. Fernando 11-18-8) and an Appeal Brief was filed on September 12, 2005.

STATUS OF CLAIMS

Claims 1-7, 9-13, and 15-17 are pending in the above-identified patent application. Claims 1-7, 9-13, and 15-17 remain rejected under 35 U.S.C. §103(a) as being unpatentable over Kaplinsky (United States Patent Number 5,298,866).

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a method and apparatus for dynamically reducing clock skew among various nodes on an integrated circuit. The disclosed clock skew reduction technique dynamically estimates the clock delay to each node and inserts a corresponding delay for each node such that the clock signals arriving at each node are all in phase with a global clock (or 180° out of phase) (page 6, line 1, to page 7, line 17). Delays attributable to both the wire RC delays and the clock buffer delays are addressed. A feedback path for the clock signal associated with each node allows the round trip travel time of the clock signal to be estimated. When the length of the feedback path matches the length of the primary clock path, the clock skew present at the corresponding node can be estimated as fifty percent (50%) of the round trip delay time (page 7, lines 10-17). Dynamic adjustments to the delay control circuit are permitted as operating conditions shift. Clock signals arriving at individual nodes on the integrated circuit remain in phase with the global PLL clock (PCK), regardless of variations in the operating voltage or temperature (or both) (page 5, lines 4-9).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-7, 9-13, and 15-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kaplinsky.

ARGUMENT

Independent Claims 1, 6 and 12

Independent claims 1, 6, and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kaplinsky. Regarding claim 1, the Examiner acknowledges that Kaplinsky does not explicitly teach that the clock delay is estimated, but asserts that Kaplinsky teaches measuring a clock delay for each of said nodes (col. 2, lines 66-67; col. 5, lines 27-28) and that it would have been obvious to a person of ordinary skill in the art to modify the teachings of Kaplinsky to estimate the clock delay instead of measuring the clock delay.

Contrary to the Examiner's assertion, Kaplinsky does not teach to ***measure*** a clock delay. Kaplinsky teaches that the output of a charge pump 69 is tuned up or down in voltage according to a digital up 67 and digital down signal 65 (FIG. 1; col. 6, line 43, to col. 7, line 2). Kaplinsky does not teach a method to set the output of the charge pump 69 at a particular value. Since the output of the charge pump 69 determines the delay time of voltage controlled delays 47, 49, the amount of delay introduced by voltage controlled delays 47, 49 is not known. Since the amount of delay introduced by voltage controlled delays 47, 49 is not known, Kaplinsky cannot measure the delay on signal paths 15 and 29. At best, Kaplinsky ***can only*** *measure the overall delay of the propagation paths*. Yet, Kaplinsky does ***not*** even disclose or suggest measuring this overall delay. Kaplinsky only compares the signal that has propagated through voltage controlled delay 47, device 11, node 33, line 15, line 29, node 35, device 37, and voltage controlled delay 49 to the signal the has propagated through voltage controlled delay 53, device 19, line 21, device 23, and voltage controlled delay 55, i.e. Kaplinsky simply compares the phase of the signals 59, 61 and determines whether to increase or decrease the output voltage of the charge pump 69 in an attempt to tune signal 61 to be in phase with signal 59.

Thus, first, the Kaplinsky statement that "the return signal lags the reference signal" "when the delay on signal paths 15 and 29 is large" (col. 6, lines 59-60) is incorrect since the relation of the return signal to the reference signal is determined by the overall delay of the propagation path and the amount of delay introduced by voltage controlled delays 47, 49. As noted above, the amount of delay introduced by voltage controlled delays 47, 49 is unknown; thus it cannot be determined whether the "lag" is the result of a large delay on signal paths 15 and 29 or a large delay by the voltage controlled delays 47, 49. Second, as noted above, Kaplinsky does ***not*** disclose or suggest measuring or estimating a clock delay for each of the nodes. Finally, Kaplinsky does ***not*** disclose or suggest adjusting the clock signal based on the estimated clock delay. Independent claims 1 and 6 require "*estimating a clock delay* and *adjusting said clock signal*...based on said *estimated clock delay*," and independent claim 12 requires a "delay driver for *adjusting said clock signal*...based on an *estimated clock delay*."

Thus, Kaplinsky does not disclose or suggest "estimating a clock delay and adjusting said clock signal...based on said estimated clock delay," as required by independent claims 1 and 6, and does not disclose or suggest a "delay driver for adjusting said clock signal...based on an estimated clock delay," as required by claim 12.

Conclusion

The rejections of the cited claims under section 103 in view Kaplinsky are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

Date: November 8, 2005

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APPENDIX

1. A method for distributing a clock signal generated by a clock generator to a plurality of nodes on an integrated circuit, said method comprising the steps of:

estimating a clock delay for each of said nodes, wherein said clock delay includes clock generator output delays and resistive-capacitive delays; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase.

2. The method of claim 1, wherein said estimating step further comprises the step of estimating a round trip delay time for said clock signals.

3. The method of claim 2, wherein said round trip delay time is obtained using a primary clock path and a return clock path.

4. The method of claim 1, wherein said integrated circuit is a system-on-chip.

5. The method of claim 1, wherein said integrated circuit is a printed circuit board.

6. A method for distributing a clock signal generated by a clock generator to a plurality of nodes on an integrated circuit, said method comprising the steps of:

providing a feedback clock path for each of said nodes, each of said feedback clock paths having an associated primary clock path that distributes said clock to each node;

determining a round trip delay time of said clock signal on each of said primary clock paths and associated feedback clock path;

estimating a clock delay for each of said nodes using said round trip travel time; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase.

7. The method of claim 6, wherein said clock delay includes a clock generator output delay and a resistive-capacitive delay.

8. (Cancelled)

9. The method of claim 6, wherein said round trip delay time is obtained using the primary clock path and a return clock path.

10. The method of claim 6, wherein said integrated circuit is a system-on-chip.

11. The method of claim 6, wherein said integrated circuit is a printed circuit board.

12. A network for distributing a clock signal generated by a clock generator to a plurality of nodes on an integrated circuit, said network comprising:

a primary clock path that distributes said clock to each node;

a feedback clock path associated with each of said primary clock paths;

a phase comparator for determining a round trip delay time of said clock signal on each of said primary clock paths and associated feedback clock path; and

a delay driver for adjusting said clock signal for each of said nodes based on an estimated clock delay for each of said nodes based on said round trip travel time, such that said clock signal arrives at each of said nodes with an aligned phase.

13. The network of claim 12, wherein said clock delay includes a clock generator output delay and a resistive-capacitive delay.

14. (Cancelled)

15. The network of claim 12, wherein said round trip delay time is obtained using the primary clock path and a return clock path.

16. The network of claim 12, wherein said integrated circuit is a system-on-chip.

17. The network of claim 12, wherein said integrated circuit is a printed circuit board.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.